Code No: R22023 **R10** SET - 1

II B. Tech II Semester Regular Examinations August - 2014
SWITCHING THEORY AND LOGIC DESIGN
(Com. to EEE, ECE, ECC, BME, EIE)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Deduce $(70.65)_8 = (\ )_2 = (\ )_{16}$
   b) Represent numeric digits 0 to 9 at least in any two self complementing codes?
   c) Explain 1's complement representation of signed number? (5M+5M+5M)

2. a) Simplify and draw the AND/OR implementations for the following switching functions?
   i) $(\overline{A}+B)(\overline{B}+C)+(AB+C)$ ii) $\overline{(A+B)}\,\overline{(ABC)}+(\overline{\overline{A}C})$
   b) Explain how hamming code is constructed for single bit error detection and correction? (8M+7M)

3. a) Find the minimum product-of-sums form for the following functions
   i) $f_1 = \prod(0, 1, 2, 3, 4, 9, 10, 13, 14)$ ii) $f_2 = AB\overline{C} + AB + C + B\overline{C} + D\overline{B}$
   b) XS3 code is used to represent the ten decimal digits. Develop the decode logic for converting from XS3 to decimal? (8M+7M)

4. a) Implement 3 bit carry-look-ahead adder, what are its advantages?
   b) Design 4 bit XS3 adder/subtractor circuit and explain the circuit operation? (8M+7M)

5. a) What is the difference between encoder and priority encoder? How do you implement decimal to BCD priority encoder?
   b) Implement the following logic functions using 8 × 1 and 4 × 1 multiplexers?
   $f(A, B, C, D) = \sum m(1, 3, 4, 6, 7, 9, 10, 11, 14)$ (7M+8M)

6. a) Draw the logic diagram to implement 16 × 8 ROM and explain its architecture?
   b) Implement 4 bit binary to gray code conversion logic functions in PLA. (7M+8M)

7. a) Explain the operation of NAND latch J-K flip-flop with preset and clear inputs?
   b) Design 4 bit twisted ring counter. Also draw its state diagram and sequence table? (8M+7M)

8. Implement the following state table using S-R flip flops (15M)

PS	inputs, x_1, x_0		
	01	10	11
A	B,0	C,1	C,0
B	A,0	D,1	D,0
C	D,0	C,0	A,1
D	C,0	A,0	D,1
	NS, Z		
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1. a) Explain how octal and hexadecimal number system is represented?
   b) Describe Excess – 3 code representation of numeric digits? What are its advantages?
   c) Subtract (– 127) from (– 115) using eight bit twos complement method? (5M+5M+5M)

2. a) How many of the input minterms are included in each of the following functions and how many are not? What are the minterm expressions for these two functions?
   i) $f_1 = A + C + BD$ ii) $f_2 = \overline{\overline{A + B} + \overline{C + D}}$
   b) Briefly describe how four bit gray code is constructed? What are its advantages? (10M+5M)

3. Minimize the following function using the Quine-McCluskey tabular method:
   $f(A, B, C, D, E) = \sum(0, 3, 4, 5, 11, 12, 13, 15)$ with don't care terms 2,6,8. (15M)

4. a) Implement a parallel adder to perform addition between two 8 bit numbers 11110011_2 and 10001101_2? Explore the result when the input carry at lowest bit is 0 and 1.
   b) Draw the logic diagram of BCD adder circuit? Explain its operation for 4 bit addition of two numbers. (8M+7M)

5. a) Explain with the help of logic diagram the operation of 3-to-8 line decoder? How such decoders are used in the realization of 1:64 de-multiplexers?
   b) A logic function has four inputs A, B, C and D that will produce output 1 whenever two adjacent input variables are 1s. Treat A and D are also adjacent. Implement this logic function using 8 × 1 and 4 × 1 multiplexers (7M+8M)

6. a) Write the programming table to implement BCD to using a PLA?
   b) Describe briefly how PAL is used to implement logic functions? Take the example of binary to BCD code conversion? (7M+8M)

7. a) Design up/down counter using J-K flip-flops to count the sequence 0, 3, 2, 6, 4, 0, …..
   b) Explain the working of 3-bit bi-directional shift register with the help of diagram? (8M+7M)

8. What are the conditions for two machines to be equivalent? For the machine given below, find the equivalence partition and corresponding reduced machine in standard form? (15M)

PS	NS, Z	
	X=0	X=1
A	F,0	B,1
B	G,0	A,1
C	B,0	C,1
D	C,0	B,1
E	D,0	A,1
F	E,1	F,1
G	E,1	G,1

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1. a) How do you convert hexadecimal fractional number into decimal number and binary number?
   b) Describe different types of numeric codes? Explain them with suitable examples? (7M+8M)

2. a) Implement the following switching functions with minimum number of NOR gates?
   i) $\left(A\overline{C}+BC\right)\left(\overline{A}+C\right)$ ii) $A\overline{B}+\left(\overline{B}+\overline{C}\right)\overline{A}$
   b) What are the different degenerative and non degenerative forms of logic gate combinations in two level realization? Briefly explain them? (8M+7M)

3. Simplify the following Boolean expression using tabulation method?
   $f\left(A, B, C, D, E\right)=\sum\left(2, 3, 4, 7, 8, 11, 13, 14\right)$ with don't care terms 1, 5, 10. (15M)

4. a) Design half subtractor? Realize full subtractor using half subtractors and explain the circuit operation?
   b) Draw the logic diagram and explain the operation of the 4 bit XS3 adder/subtractor? (7M+8M)

5. a) Obtain logical functions to design decimal to octal priority encoder? Implement the circuit with NAND gates?
   b) Implement the following Boolean function using 1 × 8 de-multiplexer and 4 × 1 multiplexer? $F\left(A, B, C\right)=\overline{A}B+AC+\overline{B}C+\overline{A}\,\overline{C}$ (7M+8M)
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6. a) How the ROM architecture is constructed? Draw structure of for 32 × 8 ROM?
   b) How the programming tables are prepared for PAL and PLA, use the following logic functions?
   i) $A(w, x, y, z) = \sum(0, 2, 5, 7, 8, 10, 12, 13)$
   ii) $B(w, x, y, z) = \sum(0, 1, 2, 6, 8, 9, 14, 15)$
   iii) $C(w, x, y, z) = \sum(0, 8, 14, 15)$ (8M+7M)

7. a) Explain the operation of J-K flip-flop? What is race around condition and how it is eliminated?
   b) Design a synchronous counter to count 3, 4, 6, 7, 3, 4, …….using J-K flip flops? (7M+8M)

8. Obtain a minimal state table using partition technique for the state table given below. Find the minimum length sequence that distinguishes state from A from state B. (15M)

PS	NS, Z	
	X=0	X=1
A	B,0	H,1
B	F,0	D,1
C	D,1	E,0
D	C,1	F,0
E	D,0	E,1
F	C,0	E,1
G	C,0	D,1
H	C,1	A,0

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1. a) Deduce *X* from the following?
   (i) $(A0.C)_{16} = (X)_8$ (ii) $(2.22)_3 = (X)_2$
   b) Briefly describe different methods of representing negative numbers? (8M+7M)

2. a) Simplify the following expressions
   i) $f_1 = (A + B + \overline{C})(A + \overline{B} + \overline{C})(\overline{A} + B + \overline{C})(\overline{A} + \overline{B} + \overline{C})$
   ii) $f_2 = A \,.\, \left[\overline{(\overline{A \oplus B}) \oplus C}\right]$
   b) What is meant by parity checking? Explain the different parity checking methods for single bit error detection and correction with suitable examples? (8M+7M)

3. a) Reduce the following expressions using Karnaugh map?
   i) $f_1 = AB + A\overline{C} + C + AD + A\overline{B}C + ABC$
   ii) $f_2 = \prod(0, 2, 8, 9, 10, 12, 13, 14)$
   b) Draw Karnaugh map and assign variables to the inputs of the AND XOR circuit shown in Figure 1, so that its output is $F(A, B, C, D) = \prod(6, 7, 12, 13)$ (8M+7M)

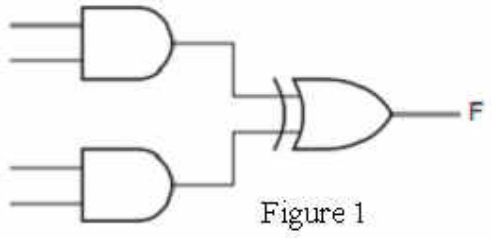

Figure 1

4. a) Describe the operation of full subtractor? Realize 4 bit binary subtractor and explain circuit operation?
   b) Design 4 bit BCD adder/subtractor and explain circuit operation with an example? (7M+8M)
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5. a) Draw the circuit diagram of 8 × 1 channel multiplexer and explain the circuit operation?
   b) Implement the following logic functions using 4-to-16-line decoder and 16 × 1 demultiplexer?
   i) $f_1 = \sum m(0, 1, 4, 7, 12, 14, 15)$
   ii) $f_2 = \sum m(1, 3, 6, 9, 12)$ (7M+8M)

6. a) What are the programmable logic devices? Explain them in brief?
   b) Obtain programmable logic to implement the following functions in PLA.
   $x(A, B, C, D) = \sum m(0, 2, 6, 7, 8, 9, 12, 13, 14)$
   $y(A, B, C, D) = \sum m(0, 3, 7, 9, 11, 12, 14)$ (7M+8M)

7. a) Describe the operation of universal shift register with the help of diagram?
   b) Design mod-9 asynchronous counter using D flip flop?
   (7M+8M)

8. Simplify the state table

PS	inputs, xy			
	xy=00	01	10	11
A	A,0	A,0	B,1	C,0
B	A,0	B,0	D,0	F,1
C	C,0	B,0	B,1	A,0
D	D,0	C,0	E,1	C,0
E	A,0	E,0	B,1	C,0
F	E,0	E,0	F,0	F,0
	NS, Z			

(15M)