SWITCHING THEORY AND LOGIC DESIGN

UNIT – I

REVIEW OF NUMBER OF SYSTEMS & CODES:

i) Representation of numbers of different radix, conversation from one radix to another radix, r-1's compliments and r's compliments of signed members, problem solving.

ii) 4 bit codes, BCD, Excess-3, 2421, 84-2-1 9's compliment code etc.,

iii) Logic operations and error detection & correction codes; Basic logic operations -NOT, OR, AND, Universal building blocks, EX-OR, EX-NOR - Gates, Standard SOP and POS, Forms, Gray code, error detection, error correction codes (parity checking, even parity, odd parity, Hamming code) NAND-NAND and NOR-NOR realizations.

UNIT – II

MINIMIZATION TECHNIQUES:

Boolean theorems, principle of complementation & duality, De-morgan theorems, minimization of logic functions using Boolean theorems, minimization of switching functions using K-Map up to 6 variables, tabular minimization, problem solving (code-converters using K-Map etc..).

UNIT – III

COMBINATIONAL LOGIC CIRCUITS DESIGN :

Design of Half adder, full adder, half subtractor, full subtractor, applications of full adders, 4-bit binary subtractor, adder-subtractor circuit, BCD adder circuit, Excess 3 adder circuit, look-a-head adder circuit, Design of decoder, demultiplexer, 7 segment decoder, higher order demultiplexing, encoder, multiplexer, higher order multiplexing, realization of Boolean functions using decoders and multiplexers, priority encoder, 4-bit digital comparator.

UNIT – IV

INTRODUCTION OF PLD's :

PROM, PAL, PLA-Basics structures, realization of Boolean function with PLDs, programming tables of PLDs, merits & demerits of PROM, PAL, PLA comparison, realization of Boolean functions using PROM, PAL, PLA, programming tables of PROM, PAL, PLA.

UNIT – V

SEQUENTIAL CIRCUITS I:

Classification of sequential circuits (synchronous and asynchronous); basic flip-flops, truth tables and excitation tables (nand RS latch, nor RS latch, RS flip-flop, JK flip-flop, T flip-flop, D flip-flop with reset and clear terminals). Conversion from one flip-flop to flip-flop. Design of ripple counters, design of synchronous counters, Johnson counter, ring counter. Design of registers - Buffer register, control buffer register, shift register, bi-directional shift register, universal shift register.

UNIT – VI

SEQUENTIAL CIRCUITS II :

Finite state machine; Analysis of clocked sequential circuits, state diagrams, state tables, reduction of state tables and state assignment, design procedures. Realization of circuits using various flip-flops. Meelay to Moore conversion and vice-versa.