Code No: L0405

Set No. 1

IV B.Tech. II Semester Regular Examinations, April 2010
DSP PROCESSORS AND ARCHITECTURES
(Common to Electronics & Communications Engineering, Electronics& Instrumentations Engineering, Bio-Medical Engineering)

Time: 3 Hours **Max Marks: 80**

Answer any Five Questions
All Questions carry equal marks
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1. a) With the aid of suitable block diagram explain the overview of a digital signal processing system. [8]
   b) What are the various types of discrete time sequences in DSP for analysis purpose and give their definitions and MATLAB representations. [8]

2. a) Describe the sources of error for evaluating the computational accuracy in DSP implementations. [8]
   b) Write notes on Compensating Filter with suitable analysis [8]

3. a) With suitable architecture explain the various data addressing capabilities for programmable DSP devices.
   b) Explain the features for external interfacing in connection with programmable DSP devices.

4. a) Explain the role of interrupts during execution process in DSP processors. [8]
   b) Explain the concept of pipelining and its performance used in DSP processors with suitable example. [8]

5. a) With relevant examples explain the data addressing modes of TMS320C54XX processors. [8]
   b) Explain the pipeline operation of TMS320C54XX processors with suitable example [8]

6. Implement a digital FIR low pass filter with the following specifications.
   $\omega_p = 0.2\pi$ $R_p = 0.25$ dB
   $\omega_s = 0.3\pi$ $A_s = 50$ dB
   Using the Parks-McClellan algorithm. Give the necessary MATLAB source code and plot the various response curves. [16]

7. a) What are the various types of FET algorithms for the efficient computation of the DFT? [8]
   b) Write notes on Butterfly Computation relevant to FET algorithms. [8]

8. a) With suitable diagram explain the concept of memory interfacing to programmable DSP devices [8]
   b) Write notes on Direct Memory Access. [8]

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Set No. 2

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Time: 3 Hours **Max Marks: 80**

Answer any Five Questions
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1. a) Define the term 'Discrete Fourier Transform' and explain its properties. [8]
   b) Consider the analog signal $x_a(t) = 3 \cos 2000 \pi t + 5 \sin 6000 \pi t + 10 \cos 12{,}000 \pi t$. [8]
   (i) What is the Nyquist rate for this signal?
   (ii) Assume now that we sample this signal using a sampling rate $F_s = 5000$ samples/sec. What is the discrete-time signal obtained after sampling?

2. a) With suitable significance explain the number formats for signals and coefficients in DSP systems. [8]
   b) Draw the circuit diagram of Compensating Filter and perform the analysis [8]

3. a) Explain the basic architectural features considered for programmable DSP devices.
   b) With suitable example explain the data addressing capabilities for programmable DSP devices. [8+8]

4. a) What is meant by 'Hardware Looping'? Explain the importance of stacks during execution process in DSP processors. [8]
   b) Explain the various interrupt effects plays a role during the execution and pipelining process in DSP processors. [8]

5. a) With relevant examples explain the memory space of TMS320C54XX processors
   b) Explain the role of on-chip peripherals for programmable digital signal processors [8+8].

6. Implement a basic DSP algorithm for digital IIR low pass filter with the following specifications.

   $\omega_p = 0.2\pi$ $R_p = 1$ dB

   $\omega_s = 0.3\pi$ $A_s = 15$ dB

   Using a Chebyshev-II prototype. Give the necessary MATLAB source code and plot the relevant response curves. [16]

7. a) Give an FET algorithm for efficient DFT computation with suitable example. [8]
   b) Write notes on Computation of the signal spectrum relevant to FET algorithms [8]

8. a) Explain the memory space organization of programmable DSP devices with simple example.
   b) Write notes on CODEC interface circuit. [8+8]

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Set No. 3

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Time: 3 Hours **Max Marks: 80**

Answer any Five Questions
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1. a) Explain the basic elements of a Digital Signal Processing system with its block diagram. [8]
   b) Explain the frequency domain representation of linear time-invariant systems. [8]

2. a) Describe the DSP Computational errors for evaluating the computational accuracy in DSP implementations [8]
   b) Differentiate A/D Conversion errors and D/A Conversion errors relevant to computational accuracy in DSP applications. [8]

3. a) Explain the various DSP Computational building blocks with the aid of its basic architecture considered for programmable DSP devices. [8]
   b) Explain the address generation unit with suitable example for programmable DSP devices. [8]

4. a) Explain the interlocking mechanism taken over during the process of pipelining in DSP processors. [8]
   b) Explain the various branching effects plays a role during the execution and pipelining process in DSP processors [8]

5. a) Explain the programming concept of TMS320C54XX processors with relevant example. [8+8]
   b) Explain the pipeline operation of TMS320C54XX processors with suitable example

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6. a) What is meant by 'Q-notation'? Differentiate FIR and IIR filters with respect to various performance parameters. [8+8]
   b) Implement direct form of adaptive FIR filter using least-mean-square algorithm.

7. a) Implement an 8-point FFT on the TMS320C54XX processor with the necessary FFT algorithm. [8+8]
   b) Write notes on overflow and scaling relevant to implementation of FET algorithms.

8. a) Explain how to interface the parallel I/O peripherals to programmable DSP devices with suitable example. [8]
   b) Write notes on multichannel buffered serial port. [8]

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Time: 3 Hours **Max Marks: 80**

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1. a) Explain how are signals processed? Briefly explain the advantages and various categories of Digital Signal Processing. [8]
   b) Explain the DSP using MATLAB with proper example [8]

2. a) Define and explain the terms 'Dynamic Range and Precision 'relevant to computational accuracy in DSP implementations. [8]
   b) Write notes on Compensating filter. [8]

3. a) Explain the bus architecture and memory organization for programmable DSP devices with relevant example. [8]
   b) Explain the speed issues and features for external interfacing for programmable DSP devices. [8]

4. a) Explain the relative branch support during the process of execution in DSP processors with suitable example. [8]
   b) Explain the various pipeline programming models that are adapted during the pipelining process in DSP processors. [8]

5. a) Explain the instructions of TMS320C54XX processors with relevant examples. [8]
   b) Explain the interrupts of TMS320C54XX processors with suitable example. [8]

6. a) Implement the interpolation filters using necessary basic DSP algorithms [8]
   b) Implement the PID Controller using the necessary DSP algorithm [8]

7. a) Explain the bit-reversed index generation with respect to FFT algorithms [8]
   b) Write notes on Butterfly computation relevant to implementation of FET algorithms [8]
8. a) Explain a CODEC interface circuit with its necessary programming by consider an example. [8]
   b) Write notes on I/O peripherals to programmable DSP devices [8]