Code No: R31041 **R10** **Set No: 1**

III B.Tech. I Semester Regular and Supplementary Examinations, January-2014
COMPUTER ARCHITECTURE & ORGANIZATION
(Com to ECE, EIE)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
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1. (a) Discuss three representations of Signed integers with suitable examples.
   (b) Explain the components of the Computer system.

2. (a) List and explain the steps involved in the execution of a complete instruction
   (b) Explain the organization of registers.

3. (a) Describe the design of hardwired control unit
   (b) Explain how microinstructions execution takes place.

4. (a) Explain the issue involved with multiplication operation.
   (b) Design 4-bit adder/Subtractor and explain its function.

5. What is a mapping function? What are the ways the cache can be mapped? Explain in detail.

6. (a) What are the steps in handling interrupts?
   (b) Explain the functions of typical input-output interface.

7. (a) Explain the advantages of symmetric multi processors over uniprocessors
   (b) Discuss the various schemes to solve the cache coherence problem.

8. Brief the following
   (a) Multi port memories.
   (b) Interprocess synchronization

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Code No: R31041 **R10** **Set No: 2**

III B.Tech. I Semester Regular and Supplementary Examinations, January-2014

COMPUTER ARCHITECTURE & ORGANIZATION

(Com to ECE, EIE)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Explain the functional architecture of the computer system.
   (b) Discuss the concept of compliments used to represent signed numbers.

2. (a) Explain instruction sequencing in detail .
   (b) Explain the various addressing modes with examples

3. Explain the basic organization of microprogrammed control unit and generation of control signals using microprogram.

4. (a) Design carry look ahead adder and explain its function.
   (b) Derive and explain an algorithm for adding and subtracting 2 floating point binary numbers

5. (a) Explain the Address Translation in Virtual Memory.
   (b) Explain different types of mapping functions in cache memory.

6. (a) How data transfers can be controlled using handshaking technique?
   (b) Discuss about Character oriented Protocol.

7. (a) Explain organization of multiprocessor system with neat sketch.
   (b) Discuss about vector operations .

8. Brief the following
   (a) Hyper cube inter connection.
   (b) Mutual exclusion with semaphore.

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Code No: R31041 **R10** **Set No: 3**

III B.Tech. I Semester Regular and Supplementary Examinations, January-2014
COMPUTER ARCHITECTURE & ORGANIZATION
(Com to ECE, EIE)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
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1. (a) Describe the connections between the processor and memory with a neat structure diagram
   (b) Find 2's complement of the following
   i) 10010 ii) 111000 iii) 0101010 iv) 111111

2. (a) What is pre-fetching? Explain how instructions can be pipelined.
   (b) With a neat diagram explain the internal organization of a processor.

3. (a) Explain micro instruction sequencing in detail.
   (b) Describe implementation of hardwired control.

4. (a) Explain hardware implementation of Binary multiplier with example.
   (b) Discuss decimal arithmetic operations.

5. (a) Explain about associative memory.
   (b) Explain internal organization of memory chips.

6. (a) With a neat sketch explain the working principle of DMA
   (b) Differentiate synchronous and asynchronous data transfer modes.

7. (a) Explain organization of NUMA with neat sketch.
   (b) How do vector processors perform matrix multiplication operations?

8. Brief the following
   (a) Time shared common bus
   (b) Serial arbitration procedure

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Code No: R31041 **R10** **Set No: 4**

III B.Tech. I Semester Regular and Supplementary Examinations, January-2014

COMPUTER ARCHITECTURE & ORGANIZATION

(Com to ECE, EIE)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Discuss about fixed point and floating point representations.
   (b) What are functions of ALU and explain.

2. (a) With examples explain the Data transfer, Logic and Program Control Instructions?
   (b) Briefly discuss about instruction format.

3. (a) Explain the Organization of the control unit to allow conditional branching in the micro program.
   (b) Mention the advantages and disadvantages of microprogrammed control hardwired control

4. (a) Explain division algorithm with example.
   (b) Explain Booth Multiplication algorithm with example.

5. (a) Analyze the memory hierarchy in terms of speed, size and Cost.
   (b) Design 64k X 16 memory chip using 16k X 8 memory chips

6. (a) What are handshaking signals. Explain the handshake control of data transfer during input and output operation
   (b) Explain the purpose of IO processors.

7. (a) Discuss Flynn taxonomy of parallel processing system.
   (b) What is Cache Coherence problem? Discuss the conditions for incoherence.

8. Brief the following
   (a) Multi stage switching network
   (b) Parallel arbitration logic

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