Code No: V3119 **R07** **Set No: 1**

III B.Tech. I Semester Supplementary Examinations, January - 2014

COMPUTER ORGANIZATION

(Common to ECE, EIE)

Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) Show the bit configuration of a 24-bit register when its content represents the Decimal Equivalent of 295: (i) in Binary (ii) in BCD (iii) in ASCII using eight bits with even parity.
   b) Perform the Subtraction with the following unsigned binary numbers by taking 2's complement of the Subtrahend (i) 11010-1101 (ii) 100-110000
   c) Explain about the Error Detection Codes with parity checker circuit. [6M+5M+5M]

2. a) Design 4–bit Combinational Circuit Decrementer using Full-adder circuits.
   b) What are the differences between a Branch Instruction, a call Subroutine Instruction and a Program Interrupt? [8M+8M]

3. a) Give the Circuit Diagram for Micro Program Sequence for a Control Memory.
   b) What is the difference between a Microprocessor and a Micro Program? [8M+8M]

4. a) With neat Flowchart, explain the Multiplication of Floating-point numbers.
   b) With the help of a Block diagram, explain the working of a BCD adder. [8M+8M]

5. a) Explain the Construction of Semiconductor Memories. Also list its advantages.
   b) Define Virtual Memory. Explain the process of converting Virtual Addresses to Physical Addresses with a neat diagram. [8M+8M]

6. a) What is Direct Memory Access (DMA)? What is the need for DMA in computers?
   b) What are the salient features of RS-232? Explain.
   c) Compare Device Polling and Daisy Chaining. [6M+5M+5M]

7. a) Explain the Flynn's Classification of Multiprocessor Systems.
   b) What is meant by Vector processing? Explain its implementation. [8M+8M]

8. a) Compare Tightly Coupled and Loosely Coupled Multiprocessor Systems.
   b) Discuss about the Shared Memory Multi Processors. [8M+8M]

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Code No: V3119 **R07** **Set No: 2**

III B.Tech. I Semester Supplementary Examinations, January - 2014

COMPUTER ORGANIZATION

(Common to ECE, EIE)

Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) Represent Decimal number 8620 in (i) BCD (ii) Excess-3 code (iii) 2421 code
   b) List the 10 BCD digits with an Even Parity in the left most position.
   c) Perform the Arithmetic Operations (+42) + (-13) and (-42) - (-13) in binary using 2's complement for negative numbers. [6M+5M+5M]

2. a) Discuss in detail about various Arithmetic Operations.
   b) Register A holds the 8-bit binary 11011001. Determine the B operand and the logic micro operation to be performed in order to change the value in A to: (i) 01101010 (ii) 11111101. [8M+8M]

3. a) Discuss in detail about Address Sequencing.
   b) Write the Symbolic Micro Program for Branch and Save Instructions. [8M+8M]

4. a) Show the Hardware required for the implementation of Booth Algorithm.
   b) Multiply 10101 with 10011 using Booth's Algorithm. [8M+8M]

5. a) Draw the Memory Hierarchy in a computer system. Explain briefly.
   b) If each Address Space represents one byte of storage space, then how many address lines are needed to access RAM chips arranged in a 4 X 6 array, where each chip is 8K X 4 bits? [8M+8M]

6. a) Describe Asynchronous Data Transfer using Strobe Control.
   b) Describe the Daisy Chaining Priority Arrangement. [8M+8M]

7. a) What is an Array Processor? Explain different types of Array Processors.
   b) Describe a 4- segment Pipeline for floating point Addition and Subtraction of two binary numbers. [8M+8M]

8. Explain the characteristics of Multiprocessor. List and explain different Interconnection Structures for Multiprocessors. [16M]

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Code No: V3119 **R07** **Set No: 3**

III B.Tech. I Semester Supplementary Examinations, January - 2014

COMPUTER ORGANIZATION

(Common to ECE, EIE)

Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) Perform the Arithmetic Operations with the decimal numbers using signed-10's complement representation for negative numbers. i) (-638) + (+785) ii) (-638) - (+185).
   b) Perform the Subtraction with the following unsigned binary numbers by taking 2's complement of the Subtrahend. (i) 11010-1101 (ii) 100-110000
   c) Explain about the Error Detection Codes with Parity Checker Circuit. [6M+6M+4M]

2. a) Explain about the One Stage of Arithmetic Logic Shift unit with a neat Diagram.
   b) Discuss in detail about the Addressing Modes. [8M+8M]

3. a) Discuss in detail about the decoding of Micro Operation fields.
   b) Show how a 9-bit Micro operation field in Microinstruction can be divided into subfields to specify 46 Micro operations? How many Micro operations can be specified in one Microinstruction? [8M+8M]

4. a) With a flow chart, explain the Multiplication of two signed-2's complement number.
   b) Derive an Algorithm in Flowchart form for Fixed Point Binary Division. [8M+8M]

5. a) Give the Merits and Demerits of different mapping Processes for Cache Organization.
   b) Describe LRU Algorithm for Page Replacement.
   c) Differentiate between Synchronous and Asynchronous DRAMs. [6M+6M+4M]

6. a) What is an I/O processor? Explain with a neat Diagram.
   b) Describe PCI Bus Structure. [8M+8M]

7. a) What is a Memory Interleaving? Compare High-order and Low-order Interleaving.
   b) What are the Applications of Vector Processing? [8M+8M]

8. What is a Cache? What is Cache Coherence? Explain its importance in Shared Memory Multiprocessor Systems? [16M]

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Code No: V3119 **R07** **Set No: 4**

III B.Tech. I Semester Supplementary Examinations, January - 2014

COMPUTER ORGANIZATION

(Common to ECE, EIE)

Time: 3 Hours **Max Marks: 80**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) Show the value of all 12-bit register that hold the number equivalent to Decimal 215 in i) Binary-Coded Decimal ii) Binary Coded Octal iii) Binary-Coded Hexadecimal.
   b) Perform the Arithmetic operations (+42) + (-13) and (-42) - (-13) in binary using 2's complement for negative numbers.
   c) List the 10 BCD digits with an Even Parity in the left most position. [6M+6M+4M]

2. a) Draw a Diagram of a Bus System for four registers using Three-state buffers and a Decoder instead of Multiplexers.
   b) Explain the Instruction Cycle with a neat Flow Chart. [8M+8M]

3. a) What is the Difference between a Microprocessor and a Micro program? Is it possible to design a Microprocessor without a Micro program?
   b) What is the function of Control Unit? Explain the difference between Hardwired control and Micro programmed control. [8M+8M]

4. a) Explain the Booth's Algorithm for Signed number Multiplication.
   b) Perform the 2's Complement Multiplication for the Signed integer operands (-13) * (-10) using Booth's recoding scheme. [8M+8M]

5. a) Draw the Block Diagram of ROM chip and explain its Operations.
   b) The access time of a Cache Memory is 100 ns and that of Main Memory is 1000 ns. It is estimated that 80% of the memory requests are found read and the remaining 20% for write. The Hit Ratio for read accesses only is 0.9. A write through process is used.
   (i) What is the average access time of the system considering only memory read cycles?
   (ii)What is the average access time of the system for both read and write requests?
   (iii) What is the Hit Ratio taking into consideration the write cycles? [6M+10M]

6. a) What is an UART? Explain the internal configuration of UART. [8M +8M]
   b) Explain the following: (i) Serial Communication (ii) Interconnected (PCI) bus.

7. What is an Instruction Pipeline? Explain, in detail, the two types of Instruction Pipeline conflicts with suitable examples. [16M]

8. a) What is a Cache Coherence problem? What are the solutions to the Cache Coherence problems?
   b) Explain the multi-port memory organization with a neat diagram. [8M +8M]

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