Set No. 1

IV (Co Time: 3	 B.Tech II Semester Regular Examinations, Apr/May 2000 EMBEDDED SYSTEMS mmon to Electrical & Electronic Engineering and Electronics Communication Engineering) hours Max Mar Answer any FIVE Questions All Questions carry equal marks ***** 	3 & ks: 80	
1. (a)	What is an embedded system? Why is it so hard to define?		
(b)	List the applications of embedded systems.	[8+8]	
2. (a)	2. (a) What is a single-purpose processor? What are the benefits of choosing a single-purpose processor to against a general-purpose processor?		
(b)	Draw the basic architecture of single-purpose processor.	[8+8]	
3. (a)	Define instruction? Explain the instruction set format?		
(b)	Explain different addressing modes with an example.	[8+8]	
4. Dra	w and explain architectural features of TMS $320C25$.	[16]	
5. (a)) What are the models commonly used for describing embedded systems?		
(b)	State differences between a computation model and a language, and a tween a textual language and a graphical language.	also be- $[8+8]$	
6. (a)	Explain how to achieve synchronization among concurrently executing p with monitors.	orocesses	
(b)	Write a solution for consumer-producer problem with monitor.	[8+8]	

- 7. Design a circuit for the expression F=abc'd'+a'cd+ab'cd with minimum gates using two level logic minimization. [16]
- 8. (a) Describe the new challenges created by cores for processor developer.
 - (b) Describe the new challenges posed by cores to processor users. [8+8]

Set No. 2

IV B.Tech II Semester Regular Examinations, Apr/May 2006 EMBEDDED SYSTEMS (Common to Electrical & Electronic Engineering and Electronics & Communication Engineering) Time: 3 hours Answer any EIVE Questions

Answer any FIVE Questions All Questions carry equal marks *****

- 1. (a) What is an embedded system? Why is it so hard to define?
 - (b) List the applications of embedded systems. [8+8]
- Design a 3-bit counter that counts the following sequence: 1,2,4,5,7,1,2,.. start from a state diagram, draw the state table, minimize the logic, and draw the final circuit.
- 3. Explain the following three application specific instruction set processors.

(a) Microcontroller

- (b) Digital signal processor
- (c) Less -general ASIP environment. [6+5+5]

4. State the need for more functional units in digital signal processor. [16]

- 5. (a) What are the models commonly used for describing embedded systems?
 - (b) State differences between a computation model and a language, and also between a textual language and a graphical language. [8+8]
- 6. (a) Describe the concurrent process model with heart beat monitoring embedded system.
 - (b) Illustrate the Set top box embedded system. [8+8]
- 7. Explain the parallel evolution of compilation and synthesis with the co-design ladder. [16]
- 8. (a) What is hardware/software co-simulation?
 - (b) What is a key method for speeding up such simulation? [8+8]

Set No. 3

IV B.Tech II Semester Regular Examinations, Apr/May 2006 EMBEDDED SYSTEMS (Common to Electrical & Electronic Engineering and Electronics & Communication Engineering)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions All Questions carry equal marks ****

- 1. (a) Using the Revenue model, derive the percentage revenue loss equations for any rise angle, rather than just for 45 degrees.
 - (b) Using the Revenue model, derive the percentage revenue loss if D=5 and W=10. [8+8]
- 2. Explain the custom single purpose processor design with GCD example. [16]
- 3. (a) Explain the factors effecting selection of a microprocessor.
 - (b) Compare the general purpose processor, microcontroller and Digital signal processor. [8+8]
- 4. Explain the architectural features of ADSP 21065. [16]
- 5. (a) Using sequential control model explain an elevator controller system.
 - (b) Define the following terms: Finite state machines, concurrent processes, real-time systems, and real-time operating systems.
- 6. (a) How to create and terminate processes.
 - (b) Explain the concept of mapping processes on processors. [8+8]
- 7. Explain the parallel evolution of compilation and synthesis with the co-design ladder. [16]
- 8. (a) What is hardware /software co-design?
 - (b) Explain temporal and spatial thinking in hardware/software co-design? [8+8]

(Common to Electrical & Electronic Engineering and Electronics &			
Time: 3 hours Max Marks: 80			
Answer any FIVE Questions All Questions carry equal marks			
* * * * *			
1.	(a) What is an embedded system? Why is it so hard to define?		
	(b) List the applications of embedded systems.	[8+8]	
2.	(a) How do NMOS and PMOS transistors differ?		
	(b) Explain the CMOS transistor working.	[8+8]	
3.	3. Explain the following three application specific instruction set processors.		
	(a) Microcontroller		
	(b) Digital signal processor		
	(c) Less -general ASIP environment.	[6+5+5]	
4.	Explain the architectural features of ADSP 21065.	[16]	
5.	(a) What are the models commonly used for describing embedded systems?		
	(b) State differences between a computation model and a language, tween a textual language and a graphical language.	and also be- $[8+8]$	
6.	(a) How to create and terminate processes.		
	(b) Explain the concept of mapping processes on processors.	[8+8]	
7.	List and describe three general approaches to improving designer proc	luctivity.[16]	
8.	Write short notes on the following:		
	(a) Instruction set simulator		
	(b) HDL simulator		

IV B.Tech II Semester Regular Examinations, Apr/May 2006 EMBEDDED SYSTEMS

Set No. 4

(c) Simulators. [6+5+5]
