USHARAMA

COLLEGE OF ENGINEERING AND TECHNOLOGY

(AUTONOMOUS)

(Approved by A.I.C.T.E & Permanently Affiliated to JNTU, Kakinada)
Accredited by NAAC with "A" Grade
on NH 16, Telaprolu, Krishna Dist – 521109

M.Tech
VLSI & Embedded Systems
Course Structure & Syllabus

(Applicable for the batches admitted from the Academic Year 2019-20)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE STRUCTURE

M.Tech – VLSI & ES
Electronics & Communication Engineering
Semester I

S.No	Course Category	Course Code	Course Title	L	T	P	Contact Hrs./wk.	Credits
1	PCC	UR19PCVE101	RTL Simulation and Synthesis with PLDs	3	0	0	3	3
2	PCC	UR19PCVE102	Microcontrollers and Programmable Digital Signal Processors	3	0	0	3	3
3	PCC	UR19PCVE103	VLSI Technology and Design	3	0	0	3	3
4	PCC	UR19PCVE104	Research Methodology and IPR	3	0	0	3	3
5	PEC		**Program Elective – I**	3	0	0	3	3
		UR19PEVE101	VLSI signal processing					
		UR19PEVE102	Digital Signal and Image Processing					
		UR19PEVE103	Parallel Processing					
6	PEC		**Program Elective – II**	3	0	0	3	3
		UR19PEVE104	Communication Networks					
		UR19PEVE105	Selected Topics in Mathematics					
		UR19PEVE106	Nano materials and Nanotechnology					
7	PCC	UR19PCVEL101	VLSI Design Lab	0	0	3	3	1.5
8	PROJ	UR19PROJVE101	Seminar – I	0	2	0	2	2
9	AD		**Audit Course – I***	0	0	0	0	0
		UR19ADVE101	English for Research Paper Writing					
		UR19ADVE102	Disaster Management					
TOTAL				**18**	**2**	**3**	**23**	**21.5**
***Internal Evaluation – Self Learning Course**								

M.Tech – VLSI & ES
Electronics & Communication Engineering
Semester II

S.No	Course Category	Course Code	Course Title	L	T	P	Contact Hrs./wk.	Credits
1	PCC	UR19PCVE201	Analog and Digital CMOS VLSI Design	3	0	0	3	3
2	PCC	UR19PCVE202	VLSI Design Verification and Testing	3	0	0	3	3
3	PCC	UR19PCVE203	Embedded System Design	3	0	0	3	3
			Program Elective – III	3	0	0	3	3
4	PEC	UR19PEVE201	Programming Languages for Embedded Software					
		UR19PEVE202	System Design with Embedded Linux					
		UR19PEVE203	CAD of Digital System					
5	PEC		**Program Elective – IV**	3	0	0	3	3
		UR19PEVE204	Memory Technologies					
		UR19PEVE205	SoC Design					
		UR19PEVE206	Low power VLSI Design					
6	PEC		**Program Elective – V**	3	0	0	3	3
		UR19PEVE207	Communication Buses and Interfaces					
		UR19PEVE208	Network Security and Cryptography.					
		UR19PEVE209	Physical design automation					
7	PCC	UR19PCVEL201	Embedded System Design Laboratory	0	0	3	3	1.5
8	PROJ	UR19PROJVE-201	Seminar – II	0	2	0	2	2
9	AD		**Audit Course – II***	0	0	0	0	0
		UR19ADVE201	Value Education					
		UR19ADVE202	Pedagogy Studies					
TOTAL				**18**	**2**	**3**	**23**	**21.5**
***Internal Evaluation – Self Learning Course**								

Semester III

S.No	Course Category	Course Code	Course Title	L	T	P	Contact Hrs./wk.	Credits
1	PROJ	UR19PROJVE301	Project Work Phase – I	0	0	20	20	10
TOTAL				**0**	**0**	**20**	**20**	**10**

Semester IV

S.No	Course Category	Course Code	Course Title	L	T	P	Contact Hrs./wk.	Credits
1	PROJ	UR19PROJVE401	Project Work Phase – II	0	0	30	30	15
TOTAL				**0**	**0**	**30**	**30**	**15**

M.Tech. I Semester **COURSE CODE: UR19PCVE101**

L	T	P	C
3	0	0	3

RTL SIMULATION AND SYNTHESIS WITH PLDS

Internal Marks: 30
External Marks: 70

Course Objectives:

1. The student will get the knowledge on design aspects of Low power VLSI design techniques.
2. To understand Design entry by Verilog/VHDL/FSM.
3. To understand Programmable Logic Devices.

UNIT I

Top down approach to design, Design of FSMs (Synchronous and asynchronous), Static timing analysis, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs.

UNIT II

Design entry by Verilog/VHDL/FSM, Verilog AMS.

UNIT III

Programmable Logic Devices, Introduction to ASIC Design Flow, FPGA, SoC, Floor planning, Placement, Clock tree synthesis, Routing, Physical verification, Power analysis, ESD protection.

UNIT IV

Design for performance, Low power VLSI design techniques, Design for testability.

UNIT V

IP and Prototyping: IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Netlist, Physical IP, Use of external hard IP during prototyping. Case studies and Speed issues.

TEXT BOOKS

1. Richard S. Sandige, “Modern Digital Design”, MGH, International Editions.
2. Donald D Givone, “Digital principles and Design”, TMH

REFERENCE BOOKS

1. Charles Roth, Jr. and Lizy K John, “Digital System Design using VHDL”, Cengage Learning.
2.Samir Palnitkar, “Verilog HDL, a guide to digital design and synthesis”, Prentice Hall.
3. Doug Amos, Austin Lesea, Rene Richter, “FPGA based prototyping methodology manual”, Xilinx.
4. Bob Zeidman, “Designing with FPGAs & CPLDs”, CMP Books.

Course Outcomes:

At the end of the course, the student will be able to

1. Familiarize with Finite State Machines, RTL design using reconfigurable logic.
2. Design and develop IP cores and Prototypes with performance guarantees.
3. Use EDA tools like Cadence, Mentor Graphics and Xilinx.
4. Synthesize digital circuits using VHDL.
5. Design and model digital circuits with Verilog HDL at behavioral, structural, and RTL Levels.
6. Design and manually optimize complex combinational and sequential digital circuits on FPGA.

M.Tech. I Semester **COURSE CODE: UR19PCVE102**

L	T	P	C
3	0	0	3

MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Internal Marks: 30
External Marks: 70

Course Objectives:

1. To Understand ARM Microcontroller operation.
2. To Understand the Programmable DSP (P-DSP) Processors.
3. To Understand the VLIW architecture and TMS320C6000 series.

UNIT I

ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces

UNIT II

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

UNIT III

LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT. Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family

UNIT IV

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations.

UNIT V

Code Composer Studio for application development for digital signal processing, On-chip peripherals, Processor benchmarking

TEXT BOOKS

1. Joseph Yiu, “The definitive guide to ARM Cortex-M3”, Elsevier, 2nd Edition
2. Venkatramani B. and Bhaskar M. “Digital Signal Processors: Architecture, Programming and Applications”, TMH, 2nd Edition

REFERENCE BOOKS

1. Sloss Andrew N, Symes Dominic, Wright Chris, “ARM System Developer's Guide: Designing and Optimizing”, Morgan Kaufman Publication
2. Steve furber, “ARM System-on-Chip Architecture”, Pearson Education
3. Frank Vahid and Tony Givargis, “Embedded System Design”, Wiley

WEB RESOURCES:

1. Technical references and user manuals on www.arm.com, NXP Semiconductor
2. www.nxp.com and Texas Instruments www.ti.com

Course Outcomes:

At the end of the course, the student will be able to

1. Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
2. Identify and characterize architecture of Programmable DSP Processors.
3. Develop small applications by utilizing the ARM processor core and DSP processor based platform.
4. Describe the Architectural features of DSP Computational building blocks.
5. Describe the Programmable Digital Signal Processors TMS320C54XX architecture.
6. Write assembly language program for microcontrollers.

M.Tech. I Semester **COURSE CODE: UR19PCVE103**

L	T	P	C
3	0	0	3

VLSI TECHNOLOGY AND DESIGN

Internal Marks: 30
External Marks: 70

Course Objectives:

1. To bring both Circuits and System views on design together.
2. It offers a profound understanding of the design of complex digital VLSI circuits, computer aided simulation and synthesis tool for hardware design.
3. To Understand Layout, Stick diagrams, Fabrication steps.

UNIT I

VLSI Technology: Fundamentals and applications, IC production process, semiconductor processes, design rules and process parameters, layout techniques and process parameters.

VLSI Design: Electronic design automation concept, ASIC and FPGA design flows, SOC designs, design technologies: combinational design techniques, sequential design techniques, state machine logic design techniques and design issues.

UNIT II

CMOS VLSI Design: MOS Technology and fabrication process of pMOS, nMOS, CMOS and BiCMOS technologies, comparison of different processes. Building Blocks of a VLSI circuit: Computer architecture, memory architectures, communication interfaces, mixed signal interfaces. VLSI Design Issues: Design process, design for testability, technology options, power calculations, package selection, clock mechanisms, mixed signal design.

UNIT III

Basic electrical properties of MOS and BiCMOS circuits: MOS and BiCMOS circuit design processes, Basic circuit concepts, scaling of MOS circuits-qualitatitive and quantitative analysis with proper illustrations and necessary derivations of expressions.

UNIT IV

Subsystem Design and Layout: Some architectural issues, switch logic, gate logic, examples of structured design (combinational logic), some clocked sequential circuits, other system considerations.

Subsystem Design Processes: Some general considerations and an illustration of design processes, design of an ALU subsystem.

UNIT V

Floor Planning: Introduction, Floor planning methods, off-chip connections.

Architecture Design: Introduction, Register-Transfer design, high-level synthesis, architectures for low power, architecture testing.

Chip Design: Introduction and design methodologies.

TEXT BOOKS

1. Essentials of VLSI Circuits and Systems, K. Eshraghian, Douglas A. Pucknell, Sholeh Eshraghian, 2005, PHI Publications.
2. Modern VLSI Design-Wayne Wolf, 3rd Ed., 1997, Pearson Education.
VLSI Design-Dr. K.V.K.K. Prasad, Kattula Shyamala, Kogent Learning Solutions Inc., 2012.

REFERENCE BOOKS

1. VLSI Design Technologies for Analog and Digital Circuits, Randall L. Geiger, Phillip E. Allen, Noel R. Strader, TMH Publications, 2010.
2. Introduction to VLSI Systems: A Logic, Circuit and System Perspective-Ming-BO Lin, CRC Press, 2011.
3. Principals of CMOS VLSI Design-N.H.E Weste, K. Eshraghian, 2nd Edition, Addison Wesley.

Course Outcomes:

At the end of the course, the student will be able to
1. Understand ASIC, FPGA and SOC design steps.
2. Design layouts for MOS circuits and analyze design rules.
3. Understand fabrication process of various MOS technologies.
4. Analyze and apply basic circuit concepts to MOS circuits.
5. Design combinational circuits, sequential circuits and sub systems.
6. Understand floor planning methods, architectural design concepts and chip design methodologies.

M.Tech. I Semester **COURSE CODE: UR19PCVE104**

L	T	P	C
3	0	0	3

RESEARCH METHODOLOGY AND IPR

Internal Marks: 30
External Marks: 70

Course Objectives:

1. To explain formulation and analysis of research problem.
2. To describe research ethics and technical writing.
3. To understand IPR and patent rights.

UNIT I

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT II

Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT III

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT IV

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

UNIT V

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS

1. Stuart Melville and Wayne Goddard, “Research methodology: an introduction for science and engineering students”.
2. Wayne Goddard and Stuart Melville, “Research Methodology: An Introduction”.

REFERENCE BOOKS

1. Ranjit Kumar, 2nd Edition, “Research Methodology: A Step by Step Guide for beginners”.
2. Halbert, “Resisting Intellectual Property”, Taylor and Francis Ltd, 2007.
3. Mayall, “Industrial Design”, McGraw Hill, 1992.
4. Niebel, “Product Design”, McGraw Hill, 1974.
5. Asimov, “Introduction to Design”, Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, “Intellectual Property in New Technological Age”, 2016.
7. T. Ramappa, “Intellectual Property Rights Under WTO”, S. Chand, 2008.

Course Outcomes:

At the end of the course, the student will be able to

1. Understand research problem formulation.
2. Analyze research related information and follow research ethics.
3. Understand that today’s world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
4. Understand that when IPR would take such important place in growth of individuals and nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general and engineering in particular.
5. Develop procedural knowledge to Legal System and solving the problem relating to intellectual property rights.
6. Establish Legal Consultancy and service provider.

M.Tech. I Semester **COURSE CODE: UR19PEVE101**

L	T	P	C
3	0	0	3

VLSI SIGNAL PROCESSING
(PE-I)

Internal Marks: 30
External Marks: 70

Course Objectives:
1. Familiarize with Pipelined and parallel processing.
2. Familiarize with Digital lattice filter structures.
3. Distinguish the various Programmable digit signal processors.

UNIT I
Introduction to DSP systems, Pipelined and parallel processing.

UNIT II
Iteration Bound, Retiming, unfolding, algorithmic strength reduction in filters and Transforms.

UNIT III
Systolic architecture design, fast convolution, pipelined and parallel recursive and adaptive filters, Scaling and round off noise.

UNIT IV
Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic.

UNIT V
Numerical strength reduction, synchronous, wave and asynchronous pipe lines, low power design, Programmable digit signal processors.

TEXT BOOK
1. Keshab K. Parthi , VLSI Digital signal processing systems, design and implementation, Wiley, Inter Science, 1999.

REFERENCE BOOKS
1. Mohammad Isamail and Terri Fiez, Analog VLSI signal and information processing, McGraw Hill, 1994
2. S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985.

Course Outcomes:
At the end of the course, the student will be able to
1. Acquire knowledge about DSP algorithms, its DFG representation, pipelining and parallel processing approaches.
2. Acquire knowledge about retiming techniques, folding and register minimization path problems.

3. Have knowledge about algorithmic strength reduction techniques and parallel.
4. Have knowledge about algorithmic strength reduction techniques and parallel Processing of FIR and IIR digital filters.
5. Acquire knowledge about finite word-length effects and round off noise computation in DSP systems.
6. Specify the applications of Programmable DSP Devices.

M.Tech. I Semester **COURSE CODE: UR19PEVE102**

L	T	P	C
3	0	0	3

DIGITAL SIGNAL AND IMAGE PROCESSING
(PE-I)

Internal Marks: 30
External Marks: 70

Course Objectives:

1. To understand the fundamental properties of Discrete Time signals and systems.
2. To develop FIR and IIR Filters.
3. To understand the Digital Image Acquisition, Enhancement and Restoration.

UNIT I

Review of Discrete Time signals and systems, Characterization in time and Z and Fourier – domain, Fast Fourier Transform algorithms – In-place computations, Butterfly computations, bit reversal's.

UNIT II

Digital Filter design: FIR - Windowing and Frequency Sampling, IIR – Impulse invariance, Bilinear Transformation.

UNIT III

Fixed point implementation of filters – challenges and techniques.

UNIT IV

Digital Image Acquisition, Enhancement, Restoration. Digital Image Coding and Compression – JPEG and JPEG 2000.

UNIT V

Color Image processing – Handling multiple planes, computational challenges. VLSI architectures for implementation of Image Processing algorithms, Pipelining.

TEXT BOOKS

1. J.G. Proakis, Manolakis "Digital Signal Processing", Pearson, 4th Edition
2. Gonzalez and Woods, "Digital Image Processing", PHI, 3rd Edition
3. S. K. Mitra. "Digital Signal Processing – A Computer based Approach", TMH, 3rd Edition, 2006

REFERENCE BOOKS

1. A.K. Jain, "Fundamentals of Digital Image Processing", Prentice Hall
2. Keshab Parhi, "VLSI Digital Signal Processing Systems – Design and Implementation", Wiley India.

Course Outcomes:

At the end of the course, the student will be able to

1. Analyze discrete-time signals and systems in various domains.
2. Design and implement filters using fixed point arithmetic targeted for embedded platforms.
3. Compare algorithmic and computational complexities in processing and coding digital images.
4. Compute various transform analysis of Linear Time Invariant System.
5. Apply engineering problem solving strategies to DSP problems.
6. Design and simulate digital filters.

M.Tech. I Semester **COURSE CODE: UR19PEVE103**

L	T	P	C
3	0	0	3

PARALLEL PROCESSING
(PE-I)

Internal Marks: 30
External Marks: 70

Course Objectives:
1. Familiarize with Overview of Parallel Processing and Pipelining.
2. Familiarize with basic concepts of VLIW processors.
3. Distinguish the various Parallel Programming Techniques.

UNIT I
Overview of Parallel Processing and Pipelining, Performance analysis, Scalability, Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining.

UNIT II
VLIW processors, Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture.

UNIT III
Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions.

UNIT IV
Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues.

UNIT V
Operating systems for multiprocessors systems, Customizing applications on parallel processing platforms.

TEXT BOOKS
1. Kai Hwang, Faye A. Briggs, “Computer Architecture and Parallel Processing”, MGH International Edition, 2009.
2. Kai Hwang, “Advanced Computer Architecture”, TMH, 2007.
3. William Stallings, “Computer Organization and Architecture, Designing for performance” Prentice Hall, Sixth edition, 2003.

REFERENCE BOOKS
1. V. Rajaraman, L. Sivaram Murthy, “Parallel Computers”, PHI.
2. Kai Hwang, Zhiwei Xu, “Scalable Parallel Computing”, MGH.
3. David Harris and Sarah Harris, “Digital Design and Computer Architecture”, Morgan Kaufmann.

Course Outcomes:

At the end of the course, the student will be able to

1. Identify limitations of different architectures of computer.
2. Analyze quantitatively the performance parameters for different architectures.
3. Investigate issues related to compilers and instruction set based on type of architectures.
4. Understand processing issues of operating systems for multiprocessor system.
5. Explain parallel and pipelining processing techniques.
6. Apply digital computers/architecture in solving real time problems as well as complex problems in industry and research.

M.Tech. I Semester **COURSE CODE: UR19PEVE104**

L	T	P	C
3	0	0	3

COMMUNICATION NETWORKS
(PE-II)

Internal Marks: 30
External Marks: 70

Course Objectives:

1. Understand state-of-the-art in network protocols, architectures, and applications.
2. Process of networking research.
3. Understand the Congestion control and Resource Allocation in networks.

UNIT I

Introduction: Network Architecture, Performance, Connecting nodes: - Connecting links, Encoding, framing, Reliable transmission, Ethernet and Multiple access networks, Wireless networks

UNIT II

Queuing models: For a) one or more servers b) with infinite and finite queue size c) Infinite population

Internetworking: Switching and bridging, IPv4, Addressing, Routing Protocols, Scale issues, Routers - Architecture, IPv6

UNIT III

End-to-End Protocols: Services, Multiplexing, De-multiplexing, UDP, TCP, RPC, RTP

UNIT IV

Congestion control and Resource Allocation: Issues, Queuing disciplines, TCP congestion control, Congestion Avoidance, QoS Applications: - Domain Name Resolution, File Transfer, Electronic Mail, WWW, Multimedia Applications

UNIT V

Network monitoring: Packet sniffing tools such as Wireshark Simulations using NS2/OPNET

TEXT BOOKS

1. Larry L. Peterson, Bruce S, Devie, “Computer Networks” , MK, 5th Edition
2. Aaron Kershenbaum, “Telecommunication Network Design Algorithms”, MGH, International Edition 1993.

REFERENCE BOOKS

1. Vijay Ahuja, “Communications Network Design and Analysis of Computer Communication Networks”, MGH, International Editions.
2. Douglas E. Comer, “Internetworking with TCP/IP”, Pearson Education, 6th Edition.

Course Outcomes:

At the end of the course, the student will be able to

1. Analyze protocols and algorithms, acknowledge tradeoffs and rationale.
2. Use routing, transport protocols for the given networking scenario and application.
3. Evaluate and develop small network applications.
4. Design a small or medium sized computer network including media types, end devices, and interconnecting devices that meets a customer's specific needs.
5. Learn to simulate computer networks and analyze the simulation results.
6. Demonstrate knowledge of programming for network communications.

M.Tech. I Semester **COURSE CODE: UR19PEVE105**

L	T	P	C
3	0	0	3

SELECTED TOPICS IN MATHEMATICS
(PE-II)

Internal Marks: 30
External Marks: 70

Course Objectives:
1. Understand the basic concept of Probability and Statistics.
2. To understand the Special Distributions.
3. To understand concepts of Graphs and Trees.

UNIT I
Probability and Statistics: Definitions, conditional probability, Baye's Theorem and independence.
Random Variables: Discrete, continuous and mixed random variables, probability mass, Probability density and cumulative distribution functions, mathematical expectation, moments, moment generating function, Chebyshev inequality.

UNIT II
Special Distributions: Discrete uniform, Binomial, Geometric, Poisson, Exponential, Gamma, Normal distributions. - Pseudo random sequence generation with given distribution, Functions of a Random Variable.

UNIT III
Joint Distributions: Joint, marginal and conditional distributions, product moments, correlation, independence of random variables, bi-variate normal distribution.
Stochastic Processes: Definition and classification of stochastic processes, Poisson process - Norms, Statistical methods for ranking data.

UNIT IV
Multivariate Data Analysis: Linear and non-linear models, Regression, Prediction and Estimation, Design of Experiments – factorial method, Response surface method.

UNIT V
Graphs and Trees: Graphs: Basic terminology, multi graphs and weighted graphs, paths and circuits, shortest path Problems, Euler and Hamiltonian paths and circuits, factors of a graph, planar graph and Kuratowski's graph and theorem, independent sets, graph colouring, Trees: Rooted trees, path length in rooted trees, binary search trees, spanning trees and cutset, theorems on spanning trees, cut sets , circuits, minimal spanning trees, Kruskal's and Prim's algorithms for minimal spanning tree.

TEXT BOOKS

1. Henry Stark, John W. Woods, “Probability and Random Process with Applications to Signal Processing”, Pearson Education, 3rd Edition
2. C. L. Liu, “Elements of Discrete Mathematics”, Tata McGraw-Hill, 2nd Edition

REFERENCE BOOKS

1. Douglas C. Montgomery, E.A. Peck and G. G. Vining, “Introduction to Linear Regression Analysis”, John Wiley and Sons, 2001.
2. Douglas C. Montgomery, “Design and Analysis of Experiments”, John Wiley and Sons, 2001.
3. B. A. Ogunnaike, “Random Phenomena: Fundamentals of Probability and Statistics for Engineers”, CRC Press, 2010.

Course Outcomes:

At the end of the course, the student will be able to

1. Characterize and represent data collected from experiments using statistical methods.
2. Model physical process/systems with multiple variables towards parameter estimation and prediction.
3. Represent systems/architectures using graphs and trees towards optimizing desired objective.
4. Apply theory of probability in identifying and solving relevant problems.
5. Show probability and expectation computations using important discrete and continuous random variable types.
6. Define function of random variable and compute density and distribution functions.

M.Tech. I Semester **COURSE CODE: UR19PEVE106**

L	T	P	C
3	0	0	3

NANO MATERIALS AND NANOTECHNOLOGY
(PE-II)

Internal Marks: 30
External Marks: 70

Course Objectives:

1. To understand the basic science behind the design and fabrication of nano scale systems.
2. To understand and formulate new engineering solutions for current problems and competing technologies for future applications.
3. To understand Interdisciplinary arena of nanotechnology.

UNIT I

Nanomaterials in one and higher dimensions.

UNIT II

Applications of one and higher dimension nano-materials.

UNIT III

Nano-lithography, micro electro-mechanical system (MEMS) and nano-phonics.

UNIT IV

Carbon Nanotubes – synthesis and applications.

UNIT V

Interdisciplinary arena of Nanotechnology.

TEXT BOOKS

1. Nanoscale Materials in Chemistry edited by Kenneth J. Klabunde and Ryan M. Richards, 2nd.edn, John Wiley and Sons, 2009.
2. Nanocrystalline Materials by A I Gusev and A ARempel, Cambridge International Science Publishing, 1st Indian edition by Viva Books Pvt. Ltd. 2008.

REFERENCE BOOKS

1. Springer Handbook of Nanotechnology by Bharat Bhushan, Springer, 3rdedn, 2010.
2. Carbon Nanotubes: Synthesis, Characterization and Applications by Kamal K. Kar, Research Publishing Services; 1stedn, 2011, ISBN-13: 978-9810863975.

Course Outcomes:

At the end of the course, the student will be able to

1. Make inter disciplinary projects applicable to wide areas by clearing and fixing the boundaries in system development.
2. Gather detailed knowledge of the operation of fabrication and characterization devices to achieve precisely designed systems.
3. Describe several synthesis methods for fabrication.
4. Consider the basic ethical, health-related and environment-related concerns encountered with respect to nanoparticles and nanomaterials in general.
5. Perform simple geometric calculations of surface energy, coordination number, and volume fraction related to nanoscale properties and synthesis, and also simple chemical calculations related to synthesis.
6. Use the acquired knowledge to evaluate which synthesis methods that can be best suited for fabricating nanostructured materials of various inorganic compounds (metals, semiconductors, oxides, fullerenes) and constructions of these.

M.Tech. I Semester **COURSE CODE: UR19PCVEL101**

L	T	P	C
0	0	3	1.5

VLSI DESIGN LAB

Internal Marks: 20
External Marks: 30

Course Objectives:
1. To design and simulation of combinational and Sequential Circuits using Mentor Graphics back end tools.
2. To familiarize concepts of 8051 programming.

PART-A: (Front-end Environment)
1. The students are required to design the logic circuit to perform the following experiments using necessary simulator (Xilinx ISE Simulator/ Mentor Graphics Questa Simulator) to verify the logical /functional operation and to perform the analysis with appropriate synthesizer (Xilinx ISE Synthesizer/Mentor Graphics Precision RTL) and then verify the implemented logic with different hardware modules/kits (CPLD/FPGA kits).
2. The students are required to acquire the knowledge in both the Platforms (Xilinx and Mentor graphics) by perform at least EIGHT experiments on each Platform.

List of Experiments:
1. Realization of Logic gates.
2. Parity Encoder.
3. Random Counter
4. Synchronous RAM.
5. ALU.
6. UART Model.
7. Fire Detection and Control System using Combinational Logic circuits.
8. Traffic Light Controller using Sequential Logic circuits
9. Pattern Detection using Moore Machine.
10. Finite State Machine (FSM) based logic circuit.

PART-B: (Back-end Environment)
The students are required to design and implement the Layout of the following experiments of any FOUR using CMOS 130nm Technology with Mentor Graphics Tool.

List of Experiments:
1. Inverter Characteristics.
2. Full Adder.

3. RS-Latch, D-Latch and Clock Divider.

4. Synchronous Counter and Asynchronous Counter.

5. Static and Dynamic RAM.

6. ROM

7. Digital-to-Analog-Converter.

8. Analog-to-Digital Converter.

Lab Requirements:

Software:

Xilinx ISE Suite 13.2 Version, Mentor Graphics-Questa Simulator, Mentor Graphics- Precision RTL, Mentor Graphics Back End/Tanner Software tool.

Hardware:

Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.

Note: Minimum 12 experiments of duration 3 periods must be completed for the eligibility to appear for the semester end examinations. In case if the student fails to get eligibility for semester end exams in the current semester, he has to take the permission of HOD and complete the required number of experiments and appear for semester end exam as and when conducted.

Course Outcomes:

At the end of the course, the student will be able to

1. Design and verify the functionality of different combinational and sequential circuits.
2. Develop and implement various digital circuits using Mentor Graphics back end Back end tools.
3. Understand and use Xilinx Vivado tools for simulation and synthesis of digital systems.
4. Design and synthesize different combinational and sequential circuits.
5. Design and implement complex digital systems using Xilinx Vivado tools.
6. Work in a team using available resources to design circuits to meet a given specification.

M.Tech. I Semester **COURSE CODE: UR19PROJVE101**

L	T	P	C
0	2	0	2

SEMINAR – I

Internal Marks: 50
External Marks: 0

The students are required to search / gather the material / information on a specific topic, comprehend it, submit report and present in the class.

Course Outcomes:

The Students will be able to

1. Understand of contemporary / emerging technology for various processes and systems.
2. Share knowledge effectively in oral and written form and formulate documents.

M.Tech. I Semester **COURSE CODE: UR19ADVE101**

L	T	P	C
0	0	0	0

ENGLISH FOR RESEARCH PAPER WRITING
(AUDIT COURSE-I)

Internal Marks: 100
External Marks: 0

Course Objectives:

1. Understand that how to improve your writing skills and level of readability.
2. Learn about what to write in each section.
3. Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission.

UNIT I

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT II

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction

UNIT III

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check., key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature

UNIT IV

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions

UNIT V

Useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

TEXT BOOKS

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books) Model Curriculum of Engineering & Technology PG Courses [Volume-I] [41]
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press

REFERENCE BOOKS

1. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book.
2. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

Course Outcomes:

At the end of the course, the student will be able to

1. Understand that how to improve writing skills and levels of readability.
2. Learn about what to write in each section.
3. Understand key skills are needed when writing a title, when writing an abstract.
4. Use Plagiarism Methods.
5. Identify what to write in each section.
6. Submit Quality Research papers.

M.Tech. I Semester **COURSE CODE: UR19ADVE102** **L T P C**
0 0 0 0

DISASTER MANAGEMENT
(AUDIT COURSE-I)

Internal Marks: 100
External Marks: 0

Course Objectives:
1. Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
2. Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
3. Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.

UNIT I
Introduction Disaster: Definition, Factors and Significance; Difference between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

UNIT II
Repercussions of Disasters and Hazards: Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

UNIT III
Disaster Prone Areas in India: Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides and Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics. Disaster Preparedness and Management Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT IV
Risk Assessment Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment, Strategies for Survival.

UNIT V
Disaster Mitigation: Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends in Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

TEXT BOOK

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company.

REFERENCE BOOKS

1. Sahni, Pardeep Et. Al. (Eds.)," Disaster Mitigation Experiences and Reflections", Prentice Hall Of India, New Delhi.
2. Goel S. L., Disaster Administration and Management Text and Case Studies", Deep & Deep Publication Pvt. Ltd., New Delhi.

Course Outcomes:

At the end of the course, the student will be able to

1. Understand key concepts in disaster risk reduction and humanitarian response.
2. Gain the knowledge destruction of echo system.
3. Know the disaster prone areas in India.
4. Explain disaster management mechanism.
5. Plan building concepts and disaster managements.
6. Understanding Disasters, man-made Hazards and Vulnerabilities.

M.Tech. II Semester **COURSE CODE: UR19PCVE201**

L	T	P	C
3	0	0	3

ANALOG AND DIGITAL CMOS VLSI DESIGN

Internal Marks: 30
External Marks: 70

Course Objectives:

1. This course covers theory and concepts to integrate both Analog and Digital CMOS design.
2. To understand the Physical design flow.
3. To understand the Single Stage Amplifier.

Digital CMOS Design:

UNIT I

Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their evaluation, Dynamic behavior, Power consumption.

UNIT II

Physical Design Flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model. Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

UNIT III

Sequential Logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit. Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, Fin FET, TFET etc.

Analog CMOS Design:

UNIT IV

Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common gate stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

UNIT V

Passive and Active Current Mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise,

Operational amplifiers: One stage OPAMP, Two stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP, Other compensation techniques.

TEXT BOOKS

1. J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2nd Edition.
2. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition.

REFERENCE BOOKS

1. Behzad Razavi , "Design of Analog CMOS Integrated Circuits", TMH, 2007.
2. Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rd Edition.
3. R J Baker, "CMOS circuit Design, Layout and Simulation", IEEE Inc., 2008.
4. Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design", TMH, 3rdEdition.
5. Pucknell, D.A. and Eshraghian, K., "Basic VLSI Design", PHI, 3rd Edition.

Course Outcomes:

At the end of the course, the student will be able to
1. Analyze, design, optimize and simulate analog and digital circuits using CMOS constrained by the design metrics.
2. Connect the individual gates to form the building blocks of a system.
3. Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Ngspice.
4. Design Sequential logic Circuits.
5. Understand Passive and active current mirrors.
6. Design and analyze Single Stage Amplifier Circuits.

M.Tech. II Semester **COURSE CODE: UR19PCVE202**

L	T	P	C
3	0	0	3

VLSI DESIGN VERIFICATION AND TESTING

Internal Marks: 30
External Marks: 70

Course Objectives:
1. To study about Verification guidelines.
2. To study about various type of data.
3. To understand the System Verilog Assertions.

UNIT I
Verification Guidelines: Verification Process, Basic Testbench functionality, directed testing, Methodology basics, Constrained-Random stimulus, Functional coverage, Testbench, components, Layered testbench, Building layered testbench, Simulation environment phases, Maximum code reuse, Testbench performance.

UNIT II
Datatypes: Built-in datatypes, Fixed-size arrays, Dynamic arrays, Queues, Associative arrays, Linked lists, Array methods, Choosing a storage type, Creating new types with typedef , Creating user-defined structures, Type conversion, Enumerated types, Constants strings, Expression width.

UNIT III
Procedural Statements and Routines: Procedural statements, tasks, functions and void functions, Routine arguments, Returning from a routine, Local data storage, Time values Connecting the testbench and design: Separating the testbench and design, Interface constructs, Stimulus timing, Interface driving and sampling, Connecting it all together, Top-level scope Program – Module interactions.

UNIT IV
System Verilog Assertions: Basic OOP: Introduction, think of nouns, Not verbs, your first class, where to define a class, OOP terminology, Creating new objects, Object de-allocation, Using objects, Static variables vs. Global variables, Class methods, Defining methods outside of the class, Scoping rules, Using one class inside another, Understanding dynamic objects, Copying objects, Public vs. Local, Straying off course building a testbench.

UNIT V
Randomization: Introduction, What to randomize, Randomization in System Verilog, Constraint details solution probabilities, Controlling multiple constraint blocks, Valid constraints, In-line constraints, The pre_randomize and post_randomize functions, Random number functions, Constraints tips and techniques, Common randomization problems, Iterative

and array constraints, Atomic stimulus generation vs. Scenario generation, Random control, Random number generators, Random device configuration.

TEXT BOOKS

1. Chris Spears, " System Verilog for Verification", Springer, 2nd Edition
2. M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers

REFERENCE BOOK

1. IEEE 1800-2009 standard (IEEE Standard for System Verilog— Unified Hardware Design, Specification, and Verification Language).

WEB RESOURCES

1. System Verilog website – www.systemverilog.org
2. http://www.sunburstdesign.com/papers/CummingsSNUG2006Boston_SystemVerilog Events.pdf
3. General reuse information and resources www.design-reuse.com
4. OVM, UVM (on top of SV) www.verificationacademy.com
5. Verification IP resources http://www.cadence.com/products/fv/verification_ip/pages/default.aspx
6. http://www.synopsys.com/Tools/Verification/FunctionalVerification/VerificationIP/Pages/default.aspx

Course Outcomes:

At the end of the course, the student will be able to

1. Familiarize with Front end design and verification techniques and create reusable test environments.
2. Verify increasingly complex designs more efficiently and effectively.
3. Use EDA tools like Cadence, Mentor Graphics.
4. Learn Testing/Debug Methods.
5. Distinguish different data types.
6. Understand Randomization.

M.Tech. II Semester **COURSE CODE: UR19PCVE203**

L	T	P	C
3	0	0	3

EMBEDDED SYSTEM DESIGN

Internal Marks: 30
External Marks: 70

Course Objectives:

1. The basic concepts of an embedded system are introduced.
2. The various elements of embedded hardware and their design principles are explained.
3. Different steps involved in the design and development of firmware for embedded systems is elaborated.

UNIT I

Introduction: An Embedded System-Definition, Examples, Current Technologies, Integration in system Design, Embedded system design flow, hardware design concepts, software development, processor in an embedded system and other hardware units, introduction to processor based embedded system design concepts.

UNIT II

Embedded Hardware: Embedded hardware building blocks, Embedded Processors – ISA architecture models, Internal processor design, processor performance, Board Memory – ROM, RAM, Auxiliary Memory, Memory Management of External Memory, Board Memory and performance. Embedded board Input / output – Serial versus Parallel I/O, interfacing the I/O components, I/O components and performance, Board buses – Bus arbitration and timing, Integrating the Bus with other board components, Bus performance.

UNIT III

Embedded Software: Device drivers, Device Drivers for interrupt-Handling, Memory device drivers, On-board bus device drivers, Board I/O drivers, Explanation about above drivers with suitable examples.

Embedded operating systems: Multitasking and process Management, Memory Management, I/O and file system management, OS standards example – POSIX, OS performance guidelines, Board support packages, Middleware and Application Software – Middle ware, Middleware examples, Application layer software examples.

UNIT IV

Embedded System Design, Development, Implementation and Testing: Embedded system design and development lifecycle model, creating an embedded system architecture, introduction to embedded software development process and tools- Host and Target machines, linking and locating software, Getting embedded software into the target system, issues in Hardware-Software design and co-design.

Implementing the design: The main software utility tool, CAD and the hardware, Translation tools, Debugging tools, testing on host machine, simulators, Laboratory tools, System Boot-Up.

UNIT V

Embedded System Design-Case Studies: Case studies- Processor design approach of an embedded system –Power PC Processor based and Micro Blaze Processor based Embedded system design on Xilinx platform-NiosII Processor based Embedded system design on Altera platform-Respective Processor architectures should be taken into consideration while designing an Embedded System.

TEXT BOOKS

1. Tammy Noergaard "Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers", Elsevier (Singapore) Pvt. Ltd. Publications, 2005.
2. Frank Vahid, Tony D. Givargis, "Embedded system Design: A Unified Hardware/Software Introduction", John Wily & Sons Inc.2002.

REFERENCE BOOKS

1. Peter Marwedel, "Embedded System Design", Science Publishers, 2007.
2. Arnold S Burger, "Embedded System Design", CMP.
3. Rajkamal, "Embedded Systems: Architecture, Programming and Design", TMH Publications, Second Edition, 2008.

Course Outcomes:

At the end of the course, the student will be able to

1. Understand the basic concepts of an embedded system.
2. Choose appropriate embedded system architecture for the given application.
3. Select the required hardware components for an embedded system and the design approach of an embedded hardware.
4. Learn about the software components required for designing an embedded system.
5. Familiarize various embedded firmware design approaches on embedded environment.
6. Write programs for optimized performance of an embedded system and validate.

M.Tech. II Semester **COURSE CODE: UR19PEVE201**

L	T	P	C
3	0	0	3

PROGRAMMING LANGUAGES FOR EMBEDDED SOFTWARE (PE-III)

Internal Marks: 30
External Marks: 70

Course Objectives:

1. To understand Embedded 'C' Programming.
2. To introduce concept of Object Oriented Programming.
3. To understand the Scripting Languages.

UNIT I

Embedded 'C' Programming: Bitwise operations, Dynamic memory allocation, OS services, Linked stack and queue, Sparse matrices, Binary tree, Interrupt handling in C, Code optimization issues, Writing LCD drives, LED drivers, Drivers for serial port communication, Embedded Software Development Cycle and Methods (Waterfall, Agile)

UNIT II

Object Oriented Programming: Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism

UNIT III

CPP Programming: 'cin', 'cout', formatting and I/O manipulators, new and delete, operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation

UNIT IV

Overloading and Inheritance: Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions.

UNIT V

Templates: Function template and class template, member function templates and template arguments,

Exception Handling: Syntax for exception handling code: try-catch- throw, Multiple Exceptions

Scripting Languages: Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing.

TEXT BOOKS

1. Michael J. Pont, “Embedded C”, Pearson Education, 2nd Edition, 2008
2. Randal L. Schwartz, “Learning Perl”, O’Reilly Publications, 6th Edition 2011

REFERENCE BOOKS

1. A. Michael Berman, “Data structures via C++”, Oxford University Press, 2002
2. Robert Sedgewick, “Algorithms in C++”, Addison Wesley Publishing Company, 1999
3. Abraham Silberschatz, Peter B, Greg Gagne, “Operating System Concepts”, John Willey & Sons, 2005

Course Outcomes:

At the end of the course, the student will be able to
1. Write an embedded C application of moderate complexity.
2. Learn Object Oriented Programming.
3. Develop and analyze algorithms in C++.
4. Understand the concepts of Overloading and Inheritance.
5. Differentiate interpreted languages from compiled languages.
6. Choose Scripting Languages depending upon the specific applications.

M.Tech. II Semester **COURSE CODE: UR19PEVE202**

L	T	P	C
3	0	0	3

SYSTEM DESIGN WITH EMBEDDED LINUX
(PE-III)

Internal Marks: 30
External Marks: 70

Course Objectives:
1. To understand embedded Linux development model.
2. To understand the Porting Applications.
3. To understand Building and Debugging.

UNIT I
Embedded Linux Vs Desktop Linux, Embedded Linux Distributions.

UNIT II
Embedded Linux, Architecture, Kernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem, IPC, User space, Start-up sequence.

UNIT III
Board Support Package, Embedded Storage: MTD, Architecture, Drivers, Embedded File System Embedded Drivers: Serial, Ethernet, I2C, USB, Timer, Kernel Modules.

UNIT IV
Porting Applications, Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux.

UNIT V
Building and Debugging: Kernel, Root file system. Embedded Graphics, Case study of uClinux.

TEXT BOOKS
1. Karim Yaghmour, “Building Embedded Linux Systems”, O'Reilly & Associates.
2. P Raghvan, Amol Lad, Sriram Neelakandan, “Embedded Linux System Design and Development”, Auerbach Publications.

REFERENCE BOOKS
1. Christopher Hallinan, “Embedded Linux Primer: A Practical Real World Approach”, Prentice Hall, 2nd Edition, 2010.
2. Derek Molloy, “Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux”, Wiley, 1st Edition, 2014.

Course Outcomes:

At the end of the course, the student will be able to

1. Appreciate the principles of the embedded Linux development model.
2. Write, debug, and profile applications and drivers in embedded Linux.
3. Understand and create Linux BSP for a hardware platform.
4. Learn the process of configuring, booting and testing the Embedded Linux distributions and applications running on Embedded Linux target systems.
5. Familiarize with Porting Applications and Real-Time Linux.
6. Acquire knowledge related to Embedded Graphics.

M.Tech. II Semester **COURSE CODE: UR19PEVE203**

L	T	P	C
3	0	0	3

CAD OF DIGITAL SYSTEM
(PE-III)

Internal Marks: 30
External Marks: 70

Course Objectives:

1. Understand the basic concept of Cryptography and Network Security, their mathematical models.
2. To understand the necessity of network security, threats/vulnerabilities to networks and countermeasures.
3. To understand Authentication functions with Message Authentication Codes and Hash Functions.

UNIT I

Introduction to VLSI Methodologies – Design and Fabrication of VLSI Devices, Fabrication Process and its impact on Design.

UNIT II

VLSI design automation tools – Data structures and basic algorithms, graph theory and computational complexity, tractable and intractable problems.

UNIT III

General purpose methods for combinational optimization – Partitioning, floor planning and pin assignment, placement, routing.

UNIT IV

Simulation – Logic synthesis, verification, high level Synthesis.

UNIT V

MCMS-VHDL-Verilog-implementation of simple circuits using VHDL

TEXT BOOK

1. N.A. Sherwani, “Algorithms for VLSI Physical Design Automation”.

REFERENCE BOOK

1. S.H. Gerez, “Algorithms for VLSI Design Automation.

Course Outcomes:

At the end of the course, the student will be able to

1. Fundamentals of CAD tools for modeling, design, test and verification of VLSI systems.
2. Study of various phases of CAD, including simulation, physical design, test and verification.
3. Demonstrate knowledge of computational algorithms and tools for CAD.
4. Size floor plan and solve routing problems.
5. Analyze different simulation and synthesis techniques.
6. Implement simple circuits using VHDL.

M.Tech. II Semester **COURSE CODE: UR19PEVE204**

L	T	P	C
3	0	0	3

MEMORY TECHNOLOGIES
(PE-IV)

Internal Marks: 30
External Marks: 70

Course Objectives:
1. To understand Random Access Memory Technologies.
2. To study the different Non-Volatile Memories.
3. To understand the concepts of Advanced Memory Technologies and High-density Memory Packing Technologies.

UNIT I
Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

UNIT II
DRAMs: DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs, SRAM and DRAM Memory controllers.

UNIT III
Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

UNIT IV
Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

UNIT V
Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices, Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging

TEXT BOOK
1. Ashok K Sharma, “Advanced Semiconductor Memories: Architectures, Designs and Applications”, Wiley Interscience

REFERENCE BOOKS

1. Kiyoo Itoh, “VLSI memory chip design”, Springer International Edition
2. Ashok K Sharma,” Semiconductor Memories: Technology, Testing and Reliability, PHI

Course outcomes:

At the end of the course, the student will be able to

1. Classify different types of RAM & ROM’s.
2. Distinguish between Static and Dynamic RAM’s.
3. Select architecture and design semiconductor memory circuits and subsystems.
4. Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
5. Learn about various Radiation Effects.
6. Know how to design state-of-the-art memory chip.

M.Tech. II Semester **COURSE CODE: UR19PEVE205**

L	T	P	C
3	0	0	3

SoC DESIGN
(PE-IV)

Internal Marks: 30
External Marks: 70

Course objectives:
1. Describe the various Overview of ASIC types.
2. To understand Different simulation modes.
3. To understand the Low power SoC design.

UNIT I
ASIC: Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

UNIT II
NISC: NISC Control Words methodology, NISC Applications and Advantages, Architecture, Description Languages (ADL) for design and verification of Application, Specific Instruction set, Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

UNIT III
Simulation: Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

UNIT IV
Low power SoC design/Digital system: Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

UNIT V
Synthesis: Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs Case study for overview of cellular phone design with emphasis on area optimization, speed improvement and power minimization.

TEXT BOOKS

1. Hubert Kaeslin, “Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication”, Cambridge University Press, 2008.
2. B. Al Hashimi, “System on chip-Next generation electronics”, The IET, 2006.

REFERENCE BOOKS

1. Rochit Rajsuman, “System-on- a-chip: Design and test”, Advantest America R & D Center, 2000.
2. P Mishra and N Dutt, “Processor Description Languages”, Morgan Kaufmann, 2008.
3. Michael J. Flynn and Wayne Luk, “Computer System Design: System-on-Chip”. Wiley, 2011.

Course Outcomes:

At the end of the course, the student will be able to

1. Identify and formulate a given problem in the framework of SoC based design approaches.
2. Design SoC based system for engineering applications.
3. Realize impact of SoC on electronic design philosophy and Macro-electronics thereby incline towards entrepreneurship & skill development.
4. Design Low power SoC.
5. Familiarize NISC Applications and Advantages.
6. Write HDL coding for minimization of power consumption.

M.Tech. II Semester **COURSE CODE: UR19PEVE206**

L	T	P	C
3	0	0	3

LOW POWER VLSI DESIGN
(PE-IV)

Internal Marks: 30
External Marks: 70

Course Objectives:
1. To understand Technology & Circuit Design Levels.
2. To understand the Logic Synthesis for Low Power estimation techniques.
3. To understand the Low Power Microprocessor Design System.

UNIT I
Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree Of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of Vdd & Vt on speed, constraints on Vt reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations.

UNIT II
Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches, Low Power Clock Distribution: Power dissipation in clock distribution, single driver Versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. Tolerable skew, chip & package co-design of clock network.

UNIT III
Logic Synthesis for Low Power Estimation Techniques: Power minimization techniques, Low power arithmetic components- circuit design styles, adders, multipliers.

UNIT IV
Low Power Memory Design: Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits.

UNIT V
Low Power Microprocessor Design System: Power management support, architectural trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance.

TEXT BOOKS
1. P. Rashinkar, Paterson and L. Singh, “Low Power Design Methodologies”, Kluwer Academic, 2002.
2. Kaushik Roy, Sharat Prasad, “Low power CMOS VLSI circuit design”, John Wiley sons Inc., 2000.

REFERENCE BOOKS

1. J. B. Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley, 1999.
2. A. P. Chandrasekaran and R. W. Broadersen, “Low power digital CMOS design”, Kluwer,1995
3. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.

Course Outcomes:

At the end of the course, the student will be able to

1. Appreciate the various techniques involved in the VLSI fabrication process.
2. Understand the different lithography methods and etching process.
3. Appreciate the deposition and diffusion mechanisms.
4. Identify the requirements for low power.
5. Distinguish static and dynamic power dissipations.
6. Identify suitable leakage power minimization technique.

M.Tech. II Semester **COURSE CODE: UR19PEVE207**

L	T	P	C
3	0	0	3

COMMUNICATION BUSSES AND INTERFACES
(PE-V)

Internal Marks: 30
External Marks: 70

Course Objectives:
1. To understand Serial Busses.
2. To understand the CIe and USB.
3. To understand the Data Streaming Serial Communication Protocol.

UNIT I
Serial Busses - Physical interface, Data and Control signals, features.

UNIT II
Limitations and applications of RS232, RS485, I2C, SPI.

UNIT III
CAN - Architecture, Data transmission, Layers, Frame formats, applications, PCIe - Revisions, Configuration space, Hardware protocols, applications.

UNIT IV
USB - Transfer types, enumeration, Descriptor types and contents, Device driver.

UNIT V
Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fiber optic and copper cable.

TEXT BOOKS
1. Jan Axelson, “Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems ”, Lakeview Research, 2nd Edition
2. Jan Axelson, “USB Complete”, Penram Publications

REFERENCE BOOKS
1. Mike Jackson, Ravi Budruk, “PCI Express Technology”, Mindshare Press.
2. Wilfried Voss, “A Comprehensible Guide to Controller Area Network”, Copperhill Media Corporation, 2nd Edition, 2005.
3. Serial Front Panel Draft Standard VITA 17.1 – 200x.

WEB RESOURCE
1. Technical references on www.can-cia.org, www.pcisig.com, www.usb.org.

Course outcomes:
At the end of the course, the student will be able to
1. Select a particular serial bus suitable for a particular application.
2. Develop APIs for configuration, reading and writing data onto serial bus.

3. Design and develop peripherals that can be interfaced to desired serial bus.
4. Describe the CAN – Architecture.
5. Classify the Transfer types of USB.
6. Explain the Data Streaming Serial Communication Protocol.

M.Tech. II Semester **COURSE CODE: UR19PEVE208**

L	T	P	C
3	0	0	3

NETWORK SECURITY AND CRYPTOGRAPHY
(PE-V)

Internal Marks: 30
External Marks: 70

Course Objectives:
1. To understand Security concepts.
2. To understand the Cryptography Techniques.
3. To understand the Authentication.

UNIT I
Security: Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.

UNIT II
Number Theory: Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

UNIT III
Private-Key (Symmetric) Cryptography: Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

UNIT IV
Public-Key (Asymmetric) Cryptography: RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

UNIT V
Authentication: IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction. System Security- Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Counter measures, Firewalls, Firewall Design Principles, Trusted Systems.

TEXT BOOKS
1. William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security,

Private Communication in a Public World", Prentice Hall, 2nd Edition.

REFERENCE BOOKS

1. Christopher M. King, Ertem Osmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Press.
2. Stephen Northcutt, Leny Zeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2nd Edition.
3. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident.

Course Outcomes:

At the end of the course, the student will be able to
1. Identify and utilize different forms of cryptography techniques.
2. Incorporate authentication and security in the network applications.
3. Distinguish among different types of threats to the system and handle the same.
4. Provide security of the data over the network.
5. Do research in the emerging areas of cryptography and network security.
6. Implement various networking protocols.

M.Tech. II Semester **COURSE CODE: UR19PEVE209**

L	T	P	C
3	0	0	3

PHYSICAL DESIGN AUTOMATION
(PE-V)

Internal Marks: 30
External Marks: 70

Course Objectives:

1. Understand the concepts of Physical Design Process such as partitioning, Floor planning, Placement and Routing.
2. Discuss the concepts of design optimization algorithms and their application to physical design automation.
3. Understand the concepts of simulation and synthesis in VLSI Design Automation.

UNIT I

Introduction to VLSI Physical Design Automation.

UNIT II

Standard cell, Performance issues in circuit layout, delay models Layout styles.

UNIT III

Discrete methods in global placement.

UNIT IV

Timing-driven placement. Global Routing Via Minimization.

UNIT V

Over the Cell Routing - Single layer and two-layer routing, Clock and Power Routing, Compaction, algorithms, Physical Design Automation of FPGAs.

TEXT BOOKS

1. S. H. Gerez, “Algorithms for VLSI Design Automation”, John Wiley, 1998.
2. N. A. Sherwani , “Algorithms for VLSI Physical Design Automation”, (3/e), Kluwer,1999.

REFERENCE BOOKS

1. S.M. Sait , H. Youssef, “VLSI Physical Design Automation”, World scientific, 1999.
2. M. Sarrafzadeh, “Introduction to VLSI Physical Design”, McGraw Hill (IE), 1996.

Course Outcomes:

At the end of the course, the student will be able to

1. Study automation process for VLSI System design.
2. Understanding of fundamentals for various physical design CAD tools.
3. Develop and enhance the existing algorithms and computational

techniques for physical design process of VLSI systems.
4. Study the basic algorithms used in layout design of VLSI circuits.
5. Learn about the physical design automation techniques used in the best-known academic and commercial layout systems.
6. Familiarize Over the Cell Routing.

M.Tech. II Semester **COURSE CODE: UR19PCVEL201**

L	T	P	C
0	0	3	1.5

EMBEDDED SYSTEM DESIGN LABORATORY

Internal Marks: 20
External Marks: 30

Course Objectives:

1. Introduce students to embedded systems design tools and hardware programmers
2. Give the students skills in both simulation and practical implementation of the basic building blocks of a microcontroller including timers, counters, PWM generation, I/O techniques and requirements, A/D conversion, serial communications

Note:

1. The Students are required to write the programs using C-Language according to the Experiment requirements using RTOS Library Functions and macros ARM-926 developer kits and ARM-Cortex.
2. The following experiments are required to develop the algorithms, flow diagrams, source code and perform the compilation, execution and implement the same using necessary hardware kits for verification. The programs developed for the implementation should be at the level of an embedded system design.
3. The students are required to perform at least EIGHT experiments from Part-I and TWO experiments from Part-II.

List of Experiments:

Part-I:

Experiments using ARM-926 with PERFECT RTOS

1. Register a new command in CLI.
2. Create a new Task.
3. Interrupt handling.
4. Allocate resource using semaphores.
5. Share resource using MUTEX.
6. Avoid deadlock using BANKER'S algorithm.
7. Synchronize two identical threads using MONITOR.
8. Reader's Writer's Problem for concurrent Tasks.

Part-II:

Experiments on ARM-CORTEX processor using any open source RTOS. (Coo-Cox-Software-Platform)

1. Implement the interfacing of display with the ARM- CORTEX processor.
2. Interface ADC and DAC ports with the Input and Output sensitive devices.

3. Simulate the temperature DATA Logger with the SERIAL communication with PC.

4. Implement the developer board as a modem for data communication using serial port communication between two PC's.

5. Relay Controller Board interfacing the ARM CORTEX Processor.

6. To interface DC motor using the ARM CORTEX Processor with PWM.

Lab Requirements:

Software:

1. Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOS Library, COO-COX Software Platform, YAGARTO TOOLS, and TFTP SERVER.
2. LINUX Environment for the compilation using Eclipse IDE & Java with latest version.

Hardware:

1. The development kits of ARM-926 Developer Kits and ARM-Cortex Boards.
2. Serial Cables, Network Cables and recommended power supply for the board.

Note: Minimum 12 experiments of duration 3 periods must be completed for the eligibility to appear for the semester end examinations. In case if the student fails to get eligibility for semester end exams in the current semester, he has to take the permission of HOD and complete the required number of experiments and appear for semester end exam as and when conducted.

Course Outcomes:

At the end of the course, the student will be able to

1. Learn fundamentals of designing embedded systems.
2. Analyze abstract problems and apply a combination of hardware and software to address the problem.
3. Design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability.
4. Make use of standard test and measurement equipment to evaluate digital interfaces.
5. Gain experience with a set of tools for embedded systems programming and debugging.
6. Read the datasheet for any embedded system, understand how it works.

M.Tech. II Semester **COURSE CODE: UR19PROJVE201**

L	T	P	C
0	2	0	2

SEMINAR – II

Internal Marks: 50
External Marks: 0

The students are required to search / gather the material / information on a specific topic, comprehend it, submit report and present in the class.

Course Outcomes:

Students will be able to

1. Understand of contemporary / emerging technology for various processes and systems.
2. Share knowledge effectively in oral and written form and formulate documents.

M.Tech. II Semester **COURSE CODE: UR19ADVE201** **L T P C**
0 0 0 0

VALUE EDUCATION
(AUDIT COURSE-II)

Internal Marks: 100
External Marks: 0

Course Objectives:
1. Understand value of education and self- development.
2. Imbibe good values in students.
3. Let them know about the importance of character.

UNIT I
Values and self-development – Social values and individual, attitudes. Work ethics, Indian vision of humanism, Moral and non- moral valuation. Standards and principles. Value judgements.

UNIT II
Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. confidence, Concentration. Truthfulness, Cleanliness.

UNIT III
Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline, Personality and Behavior Development - Soul and Scientific, attitude. Positive Thinking. Integrity and discipline. Punctuality, Love and Kindness., Avoid fault Thinking., Free from anger, Dignity of labour.

UNIT IV
Universal brotherhood and religious tolerance, True friendship, Happiness Vs suffering, love for truth, Aware of self-destructive habits, Association and Cooperation, Doing best for saving nature.

UNIT V
Character and Competence – Holy books vs Blind faith. Self-management and Good health., Science of reincarnation. Equality, Nonviolence, Humility, Role of Women, All religions and same message. Mind your Mind, Self-control. Honesty, studying effectively.

TEXT BOOK
1. Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

REFERENCE BOOK
1. Dr. N. Venkataiah, “Value Education”, A.P.H. Publishing Corporation, New Delhi 2007.

Course outcomes:

At the end of the course, the student will be able to

1. Understand the need and importance for Value Based Living.
2. Set realistic goals in life and start working towards them.
3. Realize the value of human life.
4. Emerge as responsible citizen with clear conviction to be a role-model in the society.
5. Learn the importance of Human values.
6. Developing the overall personality.

M.Tech. II Semester **COURSE CODE: UR19ADVE202**

L	T	P	C
0	0	0	0

PEDAGOGY STUDIES
(AUDIT COURSE-II)

Internal Marks: 100
External Marks: 0

Course Objectives:

1. Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
2. Identify critical evidence gaps to guide the development.

UNIT I

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology, Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions, Overview of methodology and Searching.

UNIT II

Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

UNIT III

Evidence on the effectiveness of pedagogical practices, Methodology for the in depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches., Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT IV

Professional development: alignment with classroom practices and follow-up support Peer support Support from the head teacher and the community. Curriculum and assessment Barriers to learning: limited resources and large class sizes

UNIT V

Research gaps and future directions, Research design, Contexts.

REFERENCES

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.

4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.

WEB RESOURCES

1. www.pratham.org/images/resource%20working%20paper%202.pdf

Course Outcomes:

At the end of the course, the student will be able to

1. Know pedagogical practices are being used by teachers in formal and informal classrooms in developing countries.
2. Find the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners.
3. Develop teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy.
4. Develop Overview of methodology and Searching.
5. Describe Curriculum.
6. Choose pedagogical approaches.

PROJECT WORK PHASE – I AND PHASE – II

Phase	M.Tech Semester	Course Code	L	T	P	C	Marks
I	III	UR19ECVE301	0	0	20	10	External: 100
II	IV	UR19ECVE401	0	0	30	15	

Syllabus Contents:

The project topic should be selected / chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study. The project should have the following

1. Relevance to social needs of society
2. Relevance to value addition to existing facilities in the institute
3. Relevance to industry need
4. Problems of national importance
5. Research and development in various domain

The student should complete the following:

1. Literature survey Problem Definition
2. Motivation for study and Objectives
3. Preliminary design / feasibility / modular approaches
4. Implementation and Verification
5. Report and presentation

The project phase II is based on a report prepared by the students on project topic allotted to them. It may be based on:

1. Experimental verification / Proof of concept.
2. Design, fabrication, testing of Communication System.
3. The viva-voce examination will be based on the above report and work.

Guidelines for Project Phase – I and II at M. Tech. (VLSI & ES):

1. As per the AICTE directives, the project is a yearlong activity, to be carried out and evaluated in two phases i.e. Phase – I: July to December and Phase – II: January to June.
2. The project may be carried out preferably in-house i.e. department's laboratories and centers OR in industry allotted through department's T & P coordinator.
3. After multiple interactions with guide and based on comprehensive literature survey, the student shall identify the domain and define project objectives. The referred literature should preferably include IEEE/IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Circuits-Devices and Systems, Communication-Networking and Security, Robotics and Control Systems, Signal Processing and Analysis and any other related domain. In case of Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred and reported.
4. Student is expected to detail out specifications, methodology, resources

required, critical issues involved in design and implementation and phase wise work distribution, and submit the proposal within a month from the date of registration.
5. Phase – I deliverables: A document report comprising of summary of literature survey, detailed objectives, project specifications, paper and/or computer aided design, proof of concept/functionality, part results, A record of continuous progress.
6. Phase – I evaluation: A committee comprising of guides of respective specialization shall assess the progress/performance of the student based on report, presentation and Q &A. In case of unsatisfactory performance, committee may recommend repeating the Phase-I work.
7. During phase – II, student is expected to exert on design, development and testing of the proposed work as per the schedule. Accomplished results/contributions/innovations should be published in terms of research papers in reputed journals and reviewed focused conferences OR IP/Patents.
8. Phase – II deliverables: A project report as per the specified format, developed system in the form of hardware and/or software, a record of continuous progress.
9. Phase – II evaluation: Guide along with appointed external examiner shall assess the progress/performance of the student based on report, presentation and Q &A. In case of unsatisfactory performance, committee may recommend for extension or repeating the work.

Course Outcomes:
At the end of the course, the student will be able to
1. Synthesize knowledge and skills previously gained.
2. Apply an in-depth study and execution of new technical problem.
3. Select from different methodologies, methods.
4. Form analysis to produce a suitable research design, and justify their design.
5. Present the findings of their technical solution in a written report.
6. Present the work in International/ National conference or reputed journals.